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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,522	05/29/2002	Shogo Ishioka	020239	9372

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EXAMINER

LAIR, DONALD M

ART UNIT	PAPER NUMBER
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2858

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/069,522

Applicant(s)

ISHIOKA ET AL.

Examiner

Donald M. Lair

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,2 and 4-8 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5,7 and 8 is/are rejected.
- 7) ☐ Claim(s) 6 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 March 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 4, 5, 7 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishioka et al. (US-6,703,849).

3. In regards to Claims 1 and 7, Ishioka et al. disclose an inspection apparatus for inspecting a circuit wiring on a circuit board, said inspection apparatus comprising:

supply means for supplying an electric signal to one of the ends of a circuit wiring and varying a voltage in said circuit wiring (Fig. 1, element 2);

sensor means including a plurality of sensor elements arranged in an array, each of said sensor elements being adapted to generate an inspection signal in response to voltage variation of a conductor adjacent thereto (Fig. 2, elements 11);

sensor element select means for selecting at least one sensor element adjacent to the other end of said circuit wiring among said plurality of sensor elements (Fig. 2, element 16); and

output means for outputting the inspection signal from said selected sensor element (Fig. 3, element 13),

wherein said sensor element select means includes a first switching means for controlling the connection between each of said sensor elements and the ground, and said sensor means

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includes a second switching means for controlling the connection between each of said sensor elements and said output means (Fig. 3, elements 12 – 15 and switches).

4. In regards to Claim 2, Ishioka et al. disclose the apparatus described above, wherein said supply means is adapted to supply the electric signal to selected one of a plurality of circuit wirings on said circuit board (Column 2, lines 18 – 23),

said sensor element select means is adapted to select all of the sensor elements adjacent to respective ends of said plurality of circuit wirings (Column 6, lines 9 – 12), and

when the inspection signal is generated in at least one of said sensor elements selected by said sensor element select means, said output means is adapted to output said inspection signal (Column 6, lines 12 – 23).

5. In regards to Claim 4, Ishioka et al. disclose the apparatus described above, which further includes detect means for detecting a disconnection in said circuit wiring according to the inspection signal output from said output means (Column 5, lines 55 – 63).

6. In regards to Claim 5, Ishioka et al. disclose the apparatus described above, wherein said inspection apparatuses are adapted to be disposed opposed to the circuit board (Fig. 1).

7. In regards to Claim 8, Ishioka et al. disclose the apparatus described above, wherein a plurality of circuit wirings on the circuit board are simultaneously inspected by arranging said sensor means in the plural number (Fig. 4, elements 11 and switches).

***Allowable Subject Matter***

8. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. The following is a statement of reasons for the indication of allowable subject matter:

10. The prior art of record does not disclose the apparatus described above, wherein a universal tester is adapted to be connected to the plurality of inspection apparatuses.

***Response to Arguments***

11. Applicant's arguments with respect to claims 1 – 8 have been considered but are moot in view of the new ground(s) of rejection.

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***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donald M. Lair whose telephone number is (571) 272-2232. The examiner can normally be reached on Monday - Friday, 8 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on (571) 272-2233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Donald M. Lair  
Patent Examiner  
Art Unit 2858  
April 13, 2004



**JAY PATIDAR**  
**PRIMARY EXAMINER**